REMARKS

Claims 1-60 are pending in the present application. In the Office Action, claims 40-60 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Poisner (U.S. Patent No. 6,012,154). The Examiner's rejections are respectfully traversed.

Poisner describes a watchdog timer 232 that may be used for detecting and/or recovering from computer system malfunctions. The watchdog timer 232 is located on an expansion bus bridge 230 and may periodically receive a reset signal from a software agent 212 via a host bus 220. If the watchdog timer 232 expires, and interrupt signal may be asserted to a processor 205. See Poisner, col. 4, l. 66- col.5, l. 9 and Figure 2. However, Applicant respectfully submits that Poisner does not teach or suggest determining an expiration of a watchdog timer on an integrated circuit and responding to a system error by a microcontroller on the integrated circuit, as set forth in independent claims 40, 47, and 54. To the contrary, Poisner teaches that the watchdog timer 232 is deployed on the expansion bus bridge 230, which is a completely separate device from the processor 205 and a software agent storage area 210 that stores the software agent 212.

The Examiner alleges that the limitation of an integrated circuit should not be given any patentable weight because it appears in the preamble. Applicants respectfully disagree. Independent claims 40, 47, and 54 set forth a watchdog timer on the integrated circuit and a microcontroller on the integrated circuit.

For at least the aforementioned reasons, Applicants respectfully submits that independent claims 40, 47, 54, and all claims depending therefrom are not anticipated by Poisner and request that the Examiner's rejections of claims 40-60 under 35 U.S.C. 102(b) be withdrawn.

In the Office Action, claims 1-5, 9-18, 22-31, and 35-39 were rejected under 35 U.S.C. 102(e) as being anticipated by Lindsay, et al (U.S. Patent Application Publication No. 2003/0028633). The Examiner's rejections are respectfully traversed.

Lindsay describes an ASF event controller 20 that can act to disable certain ASF functions that should not be executed in a low-power mode. For example, ASF watchdog timers 28 may be used to determine whether a device connected to a PCI bus is operating. If the device is operating, system BIOS in the device may reset the watchdog timer 28. However, if the device is not operating because of a loss of primary PCI bus power, ASF event controller 20 may set a flag 30A-B that indicates that the watchdog timer 28 should not be run. If the flag is set, the ASF firmware will not start the watchdog timer when the ASD event for this watchdog timer comes up.

The Examiner states that the ASF event controller is functionally equivalent to a microcontroller. Applicants respectfully submit that whether or not the ASF event controller is or is not functionally equivalent to a microcontroller is not material. Even if one assumes *arguendo* that the ASF event controller is a microcontroller, Lindsay does not teach or suggest a watchdog timer that is coupled to receive a reset input from a microcontroller upon a predetermined change in a system state. As discussed above, the ASF event controller 20 may set a flag, but this flag is not received by the watchdog timer described in Lindsay. Moreover, Lindsay teaches that the ASF event controller should not run the watchdog timer when the flag is set. Thus, Lindsay appears to teach that the watchdog timer should not be reset when the flag is set.

Lindsay also fails to teach or suggest providing an indication to the microcontroller in response to an expiration of the watchdog timer, as set forth in independent claims 1, 14, and 27.

Lindsay only teaches disabling the watchdog timer in response to detecting that the primary power is off.

For at least the aforementioned reasons, Applicant respectfully submits that independent claims 1, 14, 27, and all claims depending therefrom are not anticipated by Lindsay and requests that the Examiner's rejections of claims 1-5, 9-18, 22-31, and 35-39 under 35 U.S.C. 102(e) be withdrawn.

In the Office Action, claims 1-3 and 6-13, 27-29, 32-34, and 36-37 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 2-3, 5, and 8-15 of U.S. Patent Publication No. 10/067,175. Claims 27-29, 32-34, and 36-37 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 30, 32, 34, 36-38, and 40-41 of U.S. Patent Publication No. 10/067,175. In the interest of expediency, Applicant has included herein a terminal disclaimer and respectfully requests that the Examiner's rejection of claims 1-3, 6-13, 27-29, 32-34, and 36-37 be withdrawn. However, it will be appreciated that the filing of the terminal disclaimer to obviate the Examiner's rejection is not an admission of the propriety of the rejection. *Quad Environmental Technologies Corp. vs. Union Sanitary District,* 946 F.2d 870, 20 USPQ2d 1392 (Fed Cir. 1991). See, *e.g.*, MPEP §804.03.

For the aforementioned reasons, it is respectfully submitted that all claims pending in the present application are in condition for allowance. The Examiner is invited to contact the undersigned at (713) 934-4052 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

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